IN THE CLAIMS

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1 (currently amended) A driving apparatus, comprising:

an output circuit to output a differential signal;

a reference current control circuit to provide a control voltage; and

a switch circuit coupled to the output circuit to control a phase of the differential signal, [[;]] and to selectively apply the control voltage, an operational voltage, and ground to the output circuit;

~~a reference current control circuit to provide a control voltage to the output circuit such that~~ wherein a magnitude of the differential signal is determined based on at least one of a difference of the operational voltage and the control voltage and a difference of the control voltage and the ground.

2.(currently amended) The apparatus of claim 1, wherein the output circuit comprises a first transistor, a second transistor, a third transistor, and a fourth transistor, wherein the first transistor and the second transistor are directly coupled to ~~an~~ the operational voltage ~~source~~, ~~and~~ or the third transistor and the fourth transistor are directly coupled to the ground, or the first transistor and the second transistor are directly coupled to the operational voltage and the third transistor and the fourth transistor are directly coupled to the ground.

3.(original) The driving apparatus of claim 2, wherein the first transistor and the second transistor are PMOS transistors, and the third transistor and the fourth transistor are NMOS transistors.

4.(previously presented) The driving apparatus of claim 1, wherein the output circuit comprises a first transistor, a second transistor, a third transistor, and a fourth transistor, and wherein the control voltage further includes a first control voltage for controlling currents of the first transistor and the second transistor and a second control voltage for controlling currents of the third transistor and the fourth transistor.

5.(previously presented) The driving apparatus of claim 2, wherein the switch circuit is for selectively turning OFF either the first and the fourth transistors or the second and the third transistors, wherein while currents of the first and the fourth transistors are generated, the second and the third transistors are OFF, and while the first and the fourth transistors are OFF, currents of the second and the third transistors are generated.

6.(currently amended) The driving apparatus of claim 1[[5]], wherein the output circuit comprises a first transistor, a second transistor, a third transistor, and a fourth transistor, and wherein the switch circuit further comprises:

a first switch to selectively provide a first control voltage signal of the control voltage to the first transistor;

a second switch to selectively provide a second control voltage signal of the control voltage to the third transistor;

a third switch to selectively provide the first control voltage signal to the second transistor; and

a fourth switch to selectively provide the second control voltage signal to the fourth transistor;

a fifth switch to selectively provide the operational voltage ~~a third control voltage signal~~ to the first transistor;

a sixth switch to selectively provide ~~a fourth control voltage signal~~ the ground to the third transistor;

a seventh switch to selectively provide the operational voltage ~~third control voltage signal~~ to the second transistor; and

an eighth switch to selectively provide the ground ~~fourth control voltage signal~~ to the fourth transistor;

wherein the first control voltage signal is for controlling the currents of the first and the second transistors, and the second control voltage signal is for controlling the currents of the third and the fourth transistors;

wherein the operational voltage ~~third control voltage signal~~ is for turning OFF the first and the second transistors, and the ~~fourth control voltage signal~~ ground is for turning OFF the third and the fourth transistors.

7.(original) The driving apparatus of claim 6, wherein the driving apparatus further includes a switch control circuit to control the operation of the first, the second, the third, the fourth, the fifth, the sixth, the seventh, and the eighth switches.

8.(original) The driving apparatus of claim 6, wherein the first transistor and the second transistor are PMOS transistors, and the third transistor and the fourth transistor are NMOS transistors.

9.(currently amended) The driving apparatus of claim 6[[8]], wherein the operational voltage ~~third control voltage signal~~ is provided by an operational voltage source ~~and the fourth control voltage signal is provided by the ground~~.

10.(original) The driving apparatus of claim 6, wherein the first control voltage signal and the second control voltage signal are provided by the reference current control circuit.

11.(previously presented) The driving apparatus of claim 8, wherein while the second, the third, the fifth, and the eighth switches are ON, the first, the fourth, the sixth, and the seventh switches are OFF, and while the second, the third, the fifth, and the eighth switches are OFF, the first, the fourth, the sixth, and the seventh switches are ON.

12.(currently amended) A ~~The~~ driving apparatus ~~of claim 6,~~ comprising:

an output circuit to output a differential signal, the output circuit comprising a first transistor, a second transistor, a third transistor and a fourth transistor; and

a reference current control circuit to provide a control voltage to the output circuit such that a magnitude of the differential signal is determined based on the control voltage;

wherein while at least one of the currents of the first, the second, the third, the fourth transistors is generated, the at least one of the first, the second, the third, the fourth transistors operates at a saturation region.

13. (currently amended) The driving apparatus of claim [[1]]12, wherein the driving apparatus is a low voltage differential signaling (LVDS) driving apparatus.

14. (currently amended) The apparatus of claim [[1]]12, ~~wherein the output circuit comprises a first transistor, a second transistor, a third transistor, and a fourth transistor,~~ wherein the first transistor and the second transistor are directly coupled to an operational voltage source, ~~or~~ and the third transistor and the fourth transistor are directly coupled to ground ~~or both~~.

15. (original) The driving apparatus of claim 14, wherein the first transistor and the second transistor are PMOS transistors, and the third transistor and the fourth transistor are NMOS transistors.

16. (previously presented) The driving apparatus of claim 14, wherein the control voltage further includes a first control voltage for controlling currents of the first transistor and the second transistor and a second control voltage for controlling currents of the third transistor and the fourth transistor.

17. (previously presented) The driving apparatus of claim 14, wherein the switch circuit is for selectively turning OFF either the first and the fourth transistors or the second and the third transistors, wherein while currents of the first and the fourth transistors are generated, the second and the third transistors are OFF, and while

the first and the fourth transistors are OFF, currents of the second and the third transistors are generated.

18. (currently amended) The driving apparatus of claim 12, wherein the reference current control circuit comprises a current source for generating a reference current, wherein the control voltage is corresponding to the reference current.

19. (currently amended) An output circuit for outputting a differential signal, comprising:

a first transistor, coupled to an operational voltage source, having a first gate for selectively receiving ~~one of~~ a first control signal or a third control signal;

a second transistor, coupled to the operational voltage source, having a second gate for selectively receiving ~~one of~~ the first control signal or the third control signal; and

a third transistor, coupled between the first transistor and ground, having a third gate for selectively receiving ~~one of~~ a second control signal or a fourth control signal;

a fourth transistor, coupled between the ~~third~~ second transistor and the ground, having a fourth gate for selectively receiving ~~one of~~ the second control signal or the fourth control signal;

wherein the first and the second transistors are directly coupled to the operational voltage source, or the third and the fourth transistors are directly coupled to the ground, or ~~both~~ the first and the second transistors are directly coupled to the operational

voltage source and the third and the fourth transistors are directly coupled to the ground.

20. (currently amended) The output circuit of claim 19, wherein a magnitude of the differential signal is determined according to at least one of a difference of the operational voltage and the first control voltage and a difference of the second control voltage and the ground ~~while currents of the first and the fourth transistors are generated, the second and the third transistors are OFF, and while the first and the fourth transistors are OFF, currents of the second and the third transistors are generated~~.

21. (currently amended) The output circuit of claim 19, wherein a magnitude of the differential signal is determined according to at least one of the first and the second control signals.

22. (currently amended) The output circuit of claim 19[[21]], wherein while at least one of the currents of the first, the second, the third, the fourth transistors is generated, the at least one of the first, the second, the third, the fourth transistors operates at a saturation region ~~the third control signal is provided by the operational voltage source and the fourth control signal is provided by the ground~~.

23. (previously presented) The output circuit of claim 19, wherein the first and the second control signals are provided by a reference current control circuit which comprises a current source for generating a reference current, wherein the first and the second control signals are corresponding to the reference current.